

What is claimed is

1. A method of forming a SiGe layer on an insulator comprising:

providing a silicon substrate;

5 depositing a SiGe layer with a surface on the silicon substrate, whereby a Si/SiGe interface is formed;

implanting ions into the SiGe layer between the surface of the SiGe layer and the Si/SiGe interface, whereby a defect zone is formed;

10 patterning and etching the SiGe layer, whereby a patterned SiGe layer is formed; and

transferring the patterned SiGe layer to an insulator layer.

2. The method of claim 1, wherein the SiGe layer is a strained SiGe layer.

15 3. The method of claim 1, wherein the SiGe layer is a relaxed SiGe layer.

4. The method of claim 1, wherein the SiGe layer is between approximately 20nm and 1000nm thick.

20           5.     The method of claim 1, wherein the layer of SiGe has a  
Ge concentration in the range of between approximately 10% and  
60%.

          6.     The method of claim 4, wherein the layer of SiGe has a  
graded Ge concentration.

25           7.     The method of claim 4, wherein the layer of SiGe has  
an essentially constant Ge concentration.

          8.     The method of claim 1, wherein the ions comprise ions  
of hydrogen, helium, or a combination of hydrogen and argon,  
helium or boron.

30           9.     The method of claim 1, wherein the patterned SiGe  
layer comprises feature sizes between approximately 100nm and  
2cm.

35           10.    The method of claim 1, wherein transferring the  
patterned SiGe layer comprises bonding the surface of the  
patterned SiGe layer to an insulating layer on a second substrate to  
form a bonded couplet and thermally annealing the couplet to split  
the SiGe layer along the defect zone.

          11.    The method of claim 2, further comprising annealing  
the SiGe layer to relax the SiGe layer.

12. A method of forming a strained silicon film overlying  
40 an insulator comprising:  
providing a silicon substrate;  
depositing a strained SiGe layer with a surface on the  
silicon substrate, whereby a Si/SiGe interface is formed;  
implanting ions into the strained SiGe layer between  
45 the surface of the strained SiGe layer and the Si/SiGe  
interface;  
patterning and etching the strained SiGe layer,  
whereby a patterned, strained SiGe layer is formed;  
transferring the patterned, strained SiGe layer to an  
50 insulator layer;  
relaxing the strained SiGe layer, whereby the strained  
SiGe layer becomes a relaxed SiGe layer, and  
epitaxially forming a strained silicon film over the  
relaxed SiGe layer.

55 13. The method of claim 12, wherein the SiGe layer is  
between approximately 20nm and 1000nm thick.

14. The method of claim 12, wherein the layer of SiGe has  
a Ge concentration in the range of between approximately 10% and  
60%.

60 15. The method of claim 14, wherein the layer of SiGe has  
a graded Ge concentration.

16. The method of claim 14, wherein the layer of SiGe has an essentially constant Ge concentration.

65 17. The method of claim 12, wherein the ions comprise ions of hydrogen, helium, or a combination of hydrogen and argon, helium or boron.

18. The method of claim 12, wherein the patterned SiGe layer comprises feature sizes between approximately 100nm and 2cm.

70 19. The method of claim 12, wherein transferring the patterned SiGe layer comprises bonding the surface of the patterned SiGe layer to an insulating layer on a second substrate to form a bonded couplet and thermally annealing the couplet to split the SiGe layer along the defect zone

75 20. The method of claim 19, wherein relaxing the strained SiGe layer comprises additional thermal annealing.

21. A method of forming a SiGe-free strained silicon film  
on an insulator comprising:

providing a silicon substrate;

80 depositing a SiGe layer with a surface on the silicon  
substrate, whereby a Si/SiGe interface is formed;

depositing a thin epitaxial silicon layer on the surface  
of the SiGe layer;

85 implanting ions through the epitaxial silicon layer into  
the SiGe layer between the surface of the SiGe layer and the  
Si/SiGe interface;

patterning and etching epitaxial silicon layer and the  
SiGe layer, whereby a patterned Si/SiGe stack is formed;

90 transferring the patterned Si/SiGe stack to an  
insulator layer by bonding the epitaxial silicon layer to an  
insulating layer on a second substrate to form a bonded  
couplet and thermally annealing the couplet to split the SiGe  
layer along the defect zone, whereby patterned regions of  
SiGe over silicon over insulator is formed.

95 relaxing the SiGe layer, whereby the epitaxial silicon  
becomes a strained silicon film;

removing the SiGe layer.